The Creonic CCSDS AR4JA LDPC IP support the LDPC coding schemes as defined by the CCSDS standard. The LDPC codes with rates 1/2, 2/3 and 4/5, block lengths 1024, 4096 and 16384 are specially designed for deep-space missions, but the excellent error correction performance makes it the ideal fit for further applications with highest demands on forward error correction. The IP cores are available for ASIC and FPGAs (Xilinx, Intel).

CCSDS AR4JA LDPC Decoder

Key benefits of the decoder are:

- Gains of up to 3 dB compared to Viterbi decoders.
- Low-power and low-complexity design.
- Layered LDPC decoder architecture, for convergence behavior that is twice as fast as non-layered LDPC decoders
- Early stopping criterion for iterative LDPC decoder, saving a considerable amount of energy.
- Optional fixed number of iterations for fixed latency of blocks with the same code rate and block length.
- Configurable amount of LDPC decoding iterations for trading-off throughput and error correction performance.
- Collection of statistic information (number of iterations, decoding success, number of modified bits).

CCSDS AR4JA LDPC Encoder

Key benefits of the encoder are:

- High-throughput, low-latency encoder core.
- Low-power and low-complexity design.

Performance Figures

- Encoder payload throughput of up to 100 Mbit/s at 200 MHz
- Decoder payload throughput of up to more than 100 Mbit/s (30 iterations, 200 MHz)

Features

- Support for code rates 1/2, 2/3, and 4/5
- Uncoded block sizes of 1024, 4096, and 16384 bits
- Compliant with “TM Synchronization and Channel Coding, Recommended Standard, CCSDS 131.0-B-3, Blue Book, September 2017”.

Applications

- Near-Earth and Deep-Space communication.
- Space links communication.
- Space internet-working services.
- Further High-performance Applications

Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models e.g. for Aldec’s Riviera-PRO
- VHDL testbench
- bit-accurate Matlab, C or C++ simulation model
- comprehensive documentation

Error Correction Performance

The following table shows bit error rate (BER) and block error rate (BLER) of the CCSDS AR4JA LDPC decoder.

Code Rate	Block length (k)	E_b/N_0 (dB) at BER 10^{-6}	E_b/N_0 (dB) at BER 10^{-7}	E_b/N_0 (dB) at BLER 10^{-5}
1/2	1024	2.20	2.30	2.20
1/2	4096	1.60	1.65	1.60
1/2	16384	1.30	1.35	1.35
2/3	1024	2.95	3.10	3.00
2/3	4096	2.35	2.40	2.35
2/3	16384	2.05	2.10	2.05
4/5	1024	3.95	4.10	4.20
4/5	4096	3.20	3.25	3.25
4/5	16384	2.85	2.90	2.90

Error correction performance of the CCSDS AR4JA decoder at 31 iterations and 6 bit input.

Related Products

CCSDS LDPC Decoder

CCSDS SCCC Turbo Encoder and Decoder

DVB-S2X LDPC/BCH Decoder

DVB-RCS2 Turbo Decoder

About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for several algorithms of communications such as forward error correction (LDPC, Turbo, Polar), modulation, and synchronization. The company offers the richest product portfolio in this field, covering standards like 5G, 4G, DVB-S2X, DVB-RCS2, DOCSIS 3.1, WiFi, WiGig, and UWB. The products are applicable for ASIC and FPGA technology and comply with the highest requirements with respect to quality and performance. For more information please visit our website at www.creonic.com.

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