

The Creonic CCSDS LDPC IP support the LDPC coding scheme as defined by the CCSDS standard. The LDPC code with single rate 223/255 was specially designed for Near-Earth missions, but the excellent error correction performance makes it the ideal fit for further high-throughput applications. The IP cores are available for ASIC and FPGAs (Xilinx, Altera).

CCSDS LDPC Decoder

Key benefits of the decoder are:

- Gains up to 3 dB compared to Viterbi decoders.
- Low-power and low-complexity design.
- Layered LDPC decoder architecture, for twice as fast convergence behavior.
- Early stopping criterion for iterative LDPC decoder, saving a considerable amount of energy.
- Configurable amount of LDPC decoding iterations for trading-off throughput and error correction performance.
- Collection of statistic information (number of iterations, decoding success).

CCSDS LDPC Encoder

Key benefits of the encoder are:

- High-throughput, low-latency encoder core.
- Low-power and low-complexity design.
- No BRAM required.

Performance Figures

- 1.6 Gbit/s coded throughput at 200 MHz
- Decoding latency of 4.3 μ s at 5 layered decoder iterations and 200 MHz
- Encoding latency of 40 ns at 200 MHz

Features

- Support for code rate 223/255 (7136/8160)
- Coded block size 8160 bits
- Compliant with “TM Synchronization and Channel Coding, Recommended Standard, CCSDS 131.0-B-2, Blue Book, August 2011”.

Applications

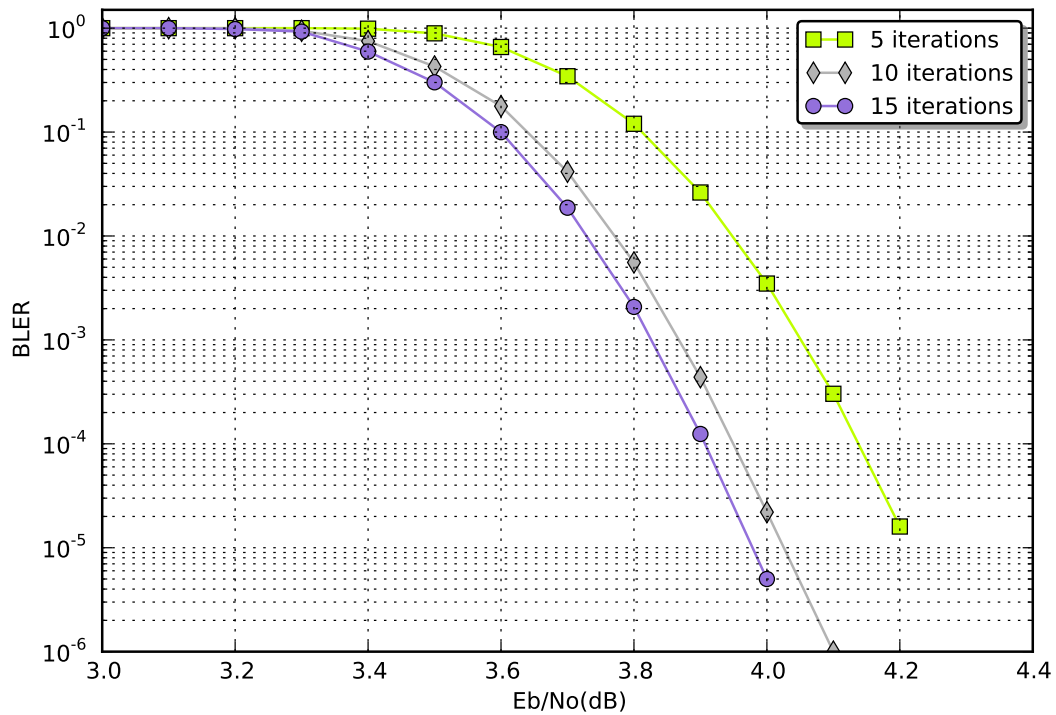
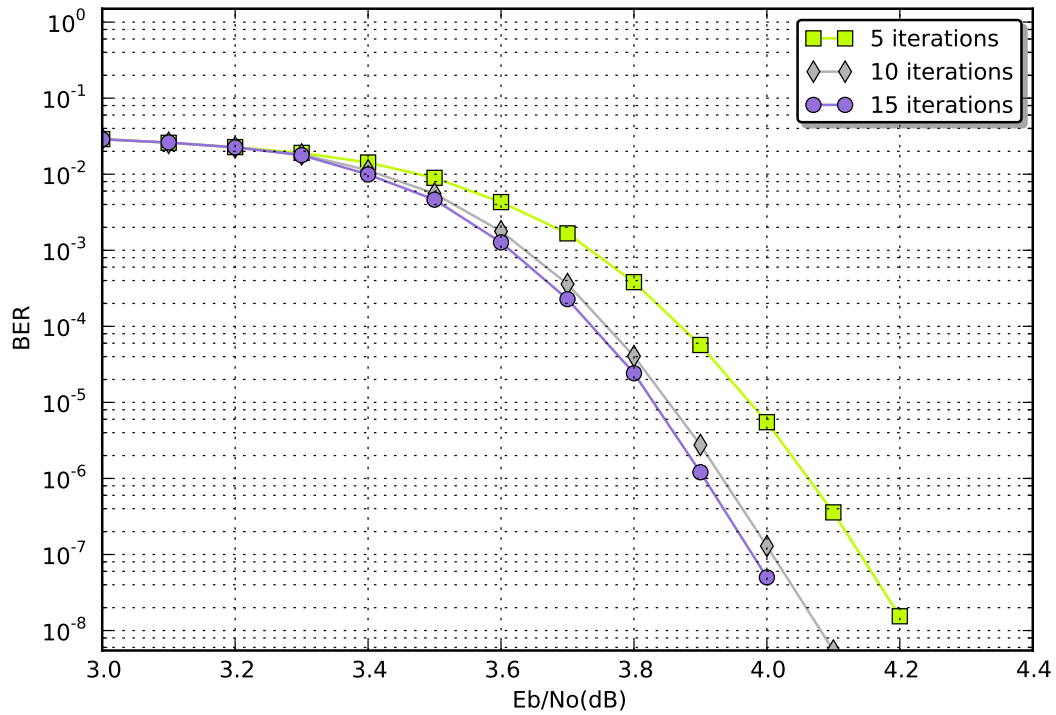
- Near-Earth and Deep-Space communication.
- Space links communication.
- Space internetworking services.
- Microwave Links
- Optical Links
- Further High-throughput Applications

Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models e.g. for Aldec’s Riviera-PRO
- VHDL or SystemC testbench
- bit-accurate Matlab, C or C++ simulation model
- comprehensive documentation

Error Correction Performance

The following figure depicts bit error rate (BER) and block error rate of the CCSDS LDPC decoder.



Related Products

[1 Gbit/s UWB LDPC Decoder](#)

[IEEE 802.11n/ac LDPC Decoder](#)

[IEEE 802.11ad LDPC Decoder](#)

[IEEE 802.11ad LDPC Decoder](#)

[IEEE 802.3bj Reed-Solomon Decoder](#)

About Creonic

Creonic is an ISO 9001:2008 certified provider of ready-for-use IP cores for several algorithms of communications such as forward error correction (LDPC and Turbo coding), synchronization, and MIMO. The company offers the richest product portfolio in this field, covering standards like DVB-S2X, LTE-A, DVB-RCS2, DOCSIS 3.1, CCSDS, WiFi, WiGig, and UWB. The products are applicable for ASIC and FPGA technology and comply with the highest requirements with respect to quality and performance. For more information, please visit www.creonic.com.

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