

Data Over Cable Service Interface Specification (DOCSIS) is an international telecommunications standard that permits the addition of high-bandwidth data transfer to an existing cable TV (CATV) system. It is employed by many cable television operators to provide Internet access over their existing hybrid fiber-coaxial infrastructure. The Creonic LDPC Decoders covers all logical channels of DOCSIS 3.1:

- The Downstream (DS) Data Decoder decodes payload data with very high throughputs.
- The PLC (Physical layer Link Channel) Decoder decodes PLC frames and therefore allows conveying the physical properties of the OFDM channel.
- The Downstream (DS) NCP (Next Codeword Pointer) Decoder decodes NCP frames and therefore allows to convey plenty of information on the OFDM structure.

## DOCSIS 3.1 Data Decoder

The Creonic DOCSIS 3.1 DS Data Decoder IP core comprises the following building blocks: zero-bits insertion unit, parity deinterleaver, LDPC decoder, zero-bits removal unit, and BCH decoder.

### Benefits

- Low-power and low-complexity design.
- Block-to-block on-the-fly configuration (iteration count, payload block size).
- Faster convergence due to layered LDPC decoder architecture.
- Early stopping criterion for iterative LDPC decoder, saving a considerable amount of energy.
- Configurable amount of LDPC decoding iterations for trading-off throughput and error correction performance.
- Collection of statistic information (number of modified information bits, number of iterations, decoding success).

### Features Data Decoder

- Parity deinterleaver, LDPC decoder, shortening unit, and BCH decoder included
- Support for all block sizes with shortening (3 to 1779 bytes payload)
- Support for data rates of more than 2.3 Gbit/s

### Features PLC Decoder

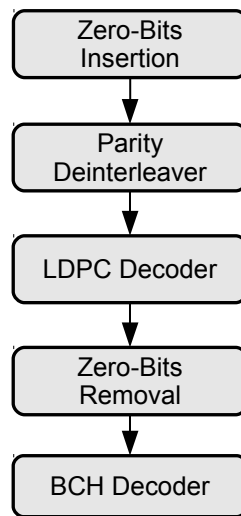
- Soft-Decision demapper, derandomizer, deinterleaver, depuncturing unit, and LDPC decoder included
- Support for 16-QAM modulation
- Support for 4k and 8k FFT size

### Features NCP Decoder

- Soft-Decision demapper, derandomizer, depuncturing unit, foreshortening unit, and LDPC decoder included
- Support for QPSK, 16-QAM and 64-QAM modulation
- Provides derandomization data for downstream data path
- Support for 4k and 8k FFT size

### Applications

- Internet services over cable TV networks.
- Wired applications with the highest demands on forward error correction.



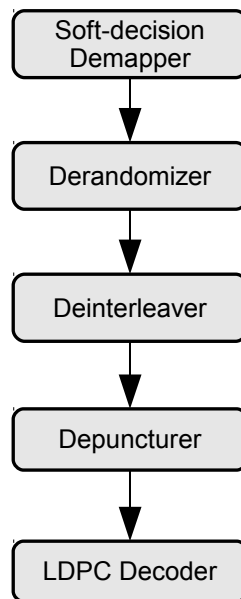
Block diagram of the DOCSIS 3.1 DS data decoder IP core.

## DOCSIS 3.1 PLC Decoder

The Creonic DOCSIS 3.1 DS PLC Decoder IP core comprises the following building blocks: soft-decision demapper, derandomizer, deinterleaver, depuncturing unit, and LDPC decoder.

### Benefits

- Low-power and low-complexity design.
  - Block-to-block on-the-fly configuration (iteration count, OFDM size).
  - Faster convergence due to layered LDPC decoder architecture.
  - Early stopping criterion for iterative LDPC decoder, saving a considerable amount of energy.
  - Configurable amount of LDPC decoding iterations for trading-off throughput and error correction performance.
  - Collection of statistic information (number of modified information bits, number of iterations, decoding success).
  - Allows for computation of modulation error ratio (MER).
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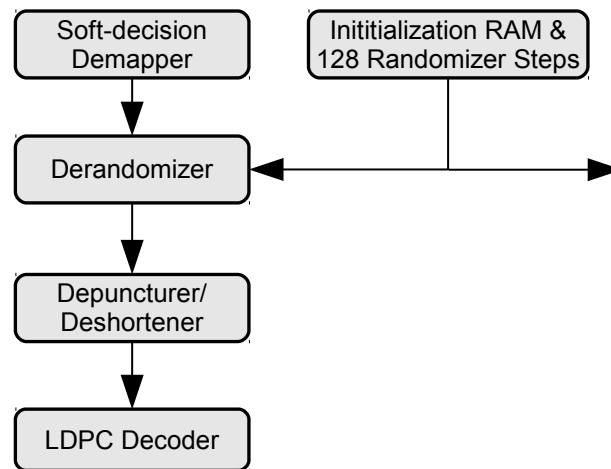
Block diagram of the DOCSIS 3.1 DS PLC decoder IP core.

## DOCSIS 3.1 NCP Decoder

The Creonic DOCSIS 3.1 DS NCP Decoder IP core comprises the following building blocks: soft-decision demapper, derandomizer, deinterleaver, depuncturing / foreshortening units, and LDPC decoder.

### Benefits

- Low-power and low-complexity design.
  - Block-to-block on-the-fly configuration (iteration count, modulation).
  - Faster convergence due to layered LDPC decoder architecture.
  - Early stopping criterion for iterative LDPC decoder, saving a considerable amount of energy.
  - Configurable amount of LDPC decoding iterations for trading-off throughput and error correction performance.
  - Collection of statistic information (number of modified information bits, number of iterations, decoding success).
  - Allows for computation of modulation error ratio (MER).
  - Provides derandomizer data for downstream data path.
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Block diagram of the DOCSIS 3.1 DS NCP decoder IP core.

## Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models e.g. for Aldec's Riviera-PRO
- VHDL testbench
- bit-accurate Matlab, C or C++ simulation model
- comprehensive documentation

## Related Products

[DVB-C2 BCH and LDPC Decoder](#)

## About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for several algorithms of communications such as forward error correction (LDPC, Turbo, Polar), modulation, and synchronization. The company offers the richest product portfolio in this field, covering standards like 5G, 4G, DVB-S2X, DVB-RCS2, DOCSIS 3.1, WiFi, WiGig, and UWB. The products are applicable for ASIC and FPGA technology and comply with the highest requirements with respect to quality and performance. For more information please visit our website at [www.creonic.com](http://www.creonic.com).

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