The Creonic Wideband Digital Down Converter (DDC) digitally converts the input signal at IF frequency down to baseband by multiplying input samples with sine/cosine waves generated by numerical controlled oscillators (NCO). Down converted samples are then decimated by a factor ranging from 2 to 2048 with multiplying step of 2. A CIC and 4 stages of half band filters are integrated within the decimator.

The core accepts a real signal at input and provides complex I/Q baseband data at the output. The parallel architecture of the core allows for an input throughput up to 2.4 Gsps, data symbol rate up to 540 Msymb/s, making it a perfect fit for ultra high throughput applications such as wideband DVB-S2X communication.

## Benefits

- Contains Numerical Controlled Oscillators, IF mixers, decimator, and halfband filters.
- High input throughput of up to 2.4 Gsps.
- Supported signal bandwidth of up to 600 MHz.
- Tunable IF frequency from 10 to 700 MHz with a precision of at least 2 Hz.
- Spurious-free dynamic range (SFDR) of at least 83 dB, filter's passband ripple less than 0.05 dB.
- Low-power and low-complexity design.
- Configurable decimation rate.
- Accepts real input signal or complex I/Q upon request.
- Memory mapped interface for configuring and retrieving status information.
- Available for ASIC and FPGAs (Xilinx, Altera).

## Features

- High throughput wideband digital down converter
- Up to 600 MHz signal bandwidth
- Tunable IF frequency
- Integrated decimator and filters

## Applications

- Wideband satellite communication
- Wideband wireless backhaul
- Wideband cable modems
- Electronic surveillance applications

## Deliverables

- VHDL source code or synthesized netlist
- VHDL testbench
- HDL simulation models
- Bit-accurate Matlab, C or C++ simulation model
- Comprehensive documentation

## Throughput

The throughput of the wideband DDC depends on the clock frequency and the sample rate (samples per symbol). The following table shows the minimum and maximum supported input and output sample rates for several clock frequencies.

| Clock frequency (MHz) | Maximum input sample rate (Msps) | Maximum output sample rate (Msps) | Maximum signal bandwidth (MHz) | Minimum symbol rate MSymb/s | Maximum symbol rate MSymb/s |
|---|---|---|---|---|---|
| 60 | 480 | 240 | 120 | 0.105 | 108.0 |
| 80 | 640 | 320 | 160 | 0.140 | 144.0 |
| 100 | 800 | 400 | 200 | 0.175 | 180.0 |
| 160 | 1280 | 640 | 320 | 0.281 | 288.0 |
| 220 | 1760 | 880 | 440 | 0.390 | 400.0 |
| 250 | 2000 | 1000 | 500 | 0.429 | 440.0 |
| 280 | 2240 | 1120 | 560 | 0.490 | 500.0 |
| 300 | 2400 | 1200 | 600 | 0.527 | 540.0 |

Minimum and maximum sample and symbol rates for different clock frequencies.

## Related Products

DVB-S2X Wideband Demodulator

DVB-S2X Wideband LDPC and BCH Decoder

DVB-S2X Wideband Modulator

## About Creonic

Creonic is an ISO 9001:2008 certified provider of ready-for-use IP cores for several algorithms of communications such as forward error correction (LDPC and Turbo coding), synchronization, and MIMO. The company offers the richest product portfolio in this field, covering standards like DVB-S2X, LTE-A, DVB-RCS2, DOCSIS 3.1, CCSDS, WiFi, WiGig, and UWB. The products are applicable for ASIC and FPGA technology and comply with the highest requirements with respect to quality and performance. For more information, please visit www.creonic.com.

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